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09/822,473	03/30/2001	Kaveh Kianush	NL 000182	8977

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EXAMINER	
NGUYEN, LEE	
ART UNIT	**PAPER NUMBER**
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/822,473
Filing Date: March 30, 2001
Appellant(s): KIANUSH ET AL.

Michael J. Ure
For Appellant

EXAMINER'S ANSWER

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

This is in response to the appeal brief filed 12/06/2004.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 1-3 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not

stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

2,148,633 MCDONALD 2-1939

Yasooka Tadashi, "Electronic frequency selection receiver", Patent Abstract of Japan, 6-1994.

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Yasooka (JP 06-125280).

Regarding claim 1, Yasooka teaches a receiver comprising RF stage 12 (fig. 1) for receiving an antenna signal from an inductive antenna 1, a processing stage 4 for processing the output signals of the RF stage and an output for supplying an audio signal 8 (fig. 1), characterized in that the RF stage comprises electronically switched capacitors 12a, 12b, controlled

by a switch control circuit 3 for adjusting front end selectivity of the RF stage to correspond to an established tuning frequency ([0011], [0017]).

Regarding claim 3, Yasooka also teaches RF stage 12 for use in a receiver (fig. 1).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yasooka in view of Macdonald (US 2,148,633) cited in the previous action.

Regarding claim 2, Yasooka fails to teach that more than two capacitors and switches are used for tuning different channels. Macdonald teaches that a plurality of capacitors and switches are used for tuning different channels (col. 2, 27-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include more capacitors and switches to the receiver of Yasooka so that more channel can be tuned.

(11) Response to Argument

Regarding the rejection of independent claim 1, the Appellant argues that Yasooka teaches manual switch, and there is no switching of capacitors under electronic control therein because the frequency

downconverter 3 is just a mixer and it does not affect the capacitors 12a and 12b.

In response, the examiner agrees that the item 3 in figures 1-2 of Yasooka is a mixer. However, item 6 which is the switch control circuit used for controlling the switching 12c of electronically switching capacitors 12a and 12b. Referring to paragraph [0020] of the translation, the frequency complement signal S1 is determined by the electronic formula frequency complement receiver of this invention turning on the frequency complement switch of said frequency complement means, and turning off, and said electronic formula frequency complement means can determine the existence of connection of tuning capacitance while choosing frequency data. In addition, referring to the abstract, Yasooka also discloses that the tuning frequency can be adjusted by changing a capacitance value by switching the number of parallel connection of the tuning capacitor by turning on/off the frequency selection switch 12c via setting the control terminal (C) of an **electronic** frequency selection means 6 at the potential when the frequency selection switch 12c is turned on. Therefore, Yasooka does teach the use of electronically switched capacitors 12a and 12b.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

LEE NGUYEN 2/17/05
Primary Examiner
Art Unit 2682

February 17, 2005

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PATENT ABSTRACTS OF JAPAN

(11)Publication number : 06-125280

(43)Date of publication of application : 06.05.1994

(51)Int.Cl. H04B 1/18

(21)Application number : 04-299369

(22)Date of filing : 12.10.1992

(71)Applicant : CITIZEN WATCH CO LTD

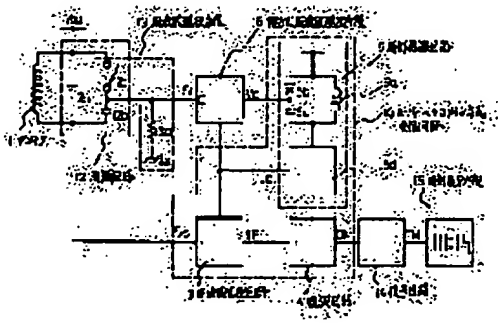
(72)Inventor : YASOOKA TADASHI

(54) ELECTRONIC FREQUENCY SELECTION RECEIVER

(57)Abstract:

PURPOSE: To perform the switching of the tuning capacitor of an antenna and that of a frequency selection means simultaneously by switching one frequency selection switch.

CONSTITUTION: A tuning frequency can be adjusted by changing a capacitance value by switching the number of parallel connection of the tuning capacitor by turning on/off the frequency selection switch 12c. and also, the frequency of an oscillator circuit 5 is selected setting potential on one terminal of the antenna 1 at the same potential as that when the frequency selection switch 12c is turned on. and setting the control terminal (c) of an electronic frequency selection means 6 at the potential when the frequency selection switch 12c is turned on.



Thereby, since the tuning capacitor can be freely selected without using a variable capacity diode, the optimum design including the antenna 1 can be performed.

LEGAL STATUS

[Date of request for examination] 05.01.1999

[Date of sending the examiner's decision of rejection] 27.11.2001

[Kind of final disposal of application other than

the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to an electronic formula frequency-selective receiver.
[0002]
[Description of the Prior Art] TERODAIN-ization is going to the supermarket of a receiving circuit in recent years with remarkable development of semiconductor technology and a microcomputer circuit technique and a rise of the frequency band used. Of course, the mobile transmitter represented by the land mobile radiotelephone is the electronic formula frequency-selective receiver of the superheterodyne method of DEJIITARU tuning of almost all receivers except for the thing of low-priced editions, such as TV, a car radio, and portable radio. PLL of the product made from SONY as an example of said electronic formula frequency-selective receiver SYNTHESIZED RECEIVERICF-SW1 is raised, and with a channel selection switch, this ICF-SW1 can carry out the numerical input of the frequency data, and can be used very conveniently.
[0003] The conventional electronic formula frequency-selective receiver is explained here using drawing 2 . Drawing 2 is the block diagram of the conventional electronic formula frequency complement receiver, and 1 connects an end to VDD which is power-source plus potential with an antenna, catches an electric-wave signal, and generates an input signal Ss. 2 is a tuning circuit, and the voltage level between anode cathodes constitutes capacity value from controllable variable-capacitance-diode 2a and tuning capacitance 2b, and where series connection of said variable-capacitance-diode 2a and tuning capacitance 2b is carried out, parallel connection is carried out to said antenna 1. And it is aligning with the tuning frequency f1 which is received frequency with the inductance value of said antenna 1, and the capacity value of a tuning circuit 2. It is the demodulator circuit which 3 considers said input signal Ss as an input, it mixes with the station dispatch number LO which is another input, and frequency conversion is carried out, it is the frequency changing circuit which outputs the intermediate frequency signal IF which is a signal of an intermediate frequency f3, and 4 inputs and detects the intermediate frequency signal IF from said frequency changing circuit 3, and outputs the recovery signal DM. 5 is a local oscillation circuit and consists of coil 5a and 5d of the oscillation sections which oscillate capacity value according to the tank constant of the tank circuit which consists of voltage levels between anode cathodes by controllable variable-capacitance-diode 5b, capacitor 5c, and said coil 5a, variable-capacitance-diode 5b and capacitor 5c. Said coil 5a connects an end to 5d of oscillation sections while connecting an end to VDD, and where series connection is carried out, parallel connection of said variable-capacitance-diode 5b and said capacitor 5c is carried out to said coil 5a. 5d of oscillation sections outputs the station dispatch number LO oscillated according to the tank constant of said tank circuit. The superheterodyne method receiving circuit 10 consists of said frequency changing circuit 3, said demodulator circuit 4, and said local oscillation circuit 5. 6 is an electronic formula frequency-selective means, and reference voltage VDD inputs VSS as a frequency-selective signal S1, and it stabilizes said control signal VC according to said frequency data by inputting said station dispatch number LO while it chooses frequency data with the logical level and outputs the

control signal VC corresponding to the frequency data. 7 is a frequency-selective means, connects an end to VDD and consists of frequency-selective switch 7a which connected the end to the control terminal C of said electronic formula frequency-selective means 6, and pull down resistor 7b which connected the end to VSS which is power-source minus potential, and connected the end to frequency-selective switch 7a. 8 changes the recovery signal DM into an audible signal by the loudspeaker.
[0004] Next, actuation of the conventional electronic formula frequency-selective receiver is explained using drawing 2 . For example, if frequency complement switch 7a of the frequency complement means 7 turns on, the frequency complement signal S1 will serve as VDD level through frequency complement switch 7a. At this time, from the logical level of said frequency complement signal S1, the electronic formula frequency complement means 6 chooses the frequency data D1, and generates a control signal VC according to these frequency data D1. Said control signal VC is supplied to the anode of variable-capacitance-diode 5b of the local oscillation circuit 5, and said variable-capacitance-diode 5b determines capacity value according to the potential difference of VDD supplied to a cathode, and the control signal VC supplied to an anode. And from the tank constant of said variable-capacitance-diode 5b, capacitor 5c, and coil 5a, the oscillation frequency of the local oscillation circuit 5 is decided, and it is outputted as a station dispatch number LO. Said electronic formula frequency-selective means 6 compares the frequency and said frequency data D1 of the station dispatch number LO by inputting said station dispatch number LO here. By lowering the potential of said control signal VC, if the frequency f2 of the station dispatch number LO is lower than the frequency of the frequency data D1 It controls in the direction which enlarges the cathode of said variable-capacitance-diode 5b, and the potential difference of an anode, and it controls so that capacity value is made small and the oscillation frequency of the local oscillation circuit 5 becomes high. Moreover, if the frequency f2 of the station dispatch number LO is higher than the frequency of the frequency data D1, by raising the potential of said control signal VC, it will control in the direction which makes small the cathode of said variable-capacitance-diode 5b, and the potential difference of an anode, and it will control so that capacity value is enlarged and the oscillation frequency of the local oscillation circuit 5 becomes low. Thus, by being controlled to be stabilized in accordance with the frequency data D1 of the electronic formula frequency complement means 6, the frequency f2 from a station of the station dispatch number LO of the local oscillation circuit 5 can supply the very accurate local oscillation circuit 5. Moreover, said control signal VC is supplied also to the anode of said variable-capacitance-diode 2a of said tuning circuit 2, variable-capacitance-diode 2a determines capacity value according to the potential difference of the cathode in the potential level of VDD, and the anode in the potential level of a control signal VC, and tuning frequency f1 is decided by the capacity value of said tuning capacitance 2b adjusted beforehand, and the inductance of said antenna 1. The frequency f2 from a station and said tuning frequency f1 of said station dispatch number LO always have an intermediate frequency f3 and the relation of a degree type here. f3=f2-f1. Therefore, it depends for tuning frequency f1 on said frequency data D1.
[0005] The electric-wave signal of the tuning frequency f1 efficiently received by said antenna 1 and tuning circuit 2 is inputted into said frequency changing circuit 3 as an input signal Ss. By the frequency changing circuit 3, on the frequency f2 of said station dispatch number LO, frequency conversion of said input signal Ss is carried out, and it is outputted as said intermediate frequency signal IF of an intermediate frequency f3, and it is detected in said demodulator circuit 4 designed only for [of an intermediate frequency f3] detection, and is outputted as a recovery signal DM. This is the description of the superheterodyne method receiving circuit 10 which was excellent in the recovery engine performance. Said recovery signal DM is pronounced as an audible signal by said loudspeaker 8.
[0006] In the conventional electronic formula frequency complement receiver, the superheterodyne method receiving circuit 10 which was excellent in the recovery engine performance is realized as mentioned above by being able to perform received frequency alignment automatically and having the local oscillation circuit 5 by which precision was stabilized very much well by switch of easy frequency complement switch 7a of actuation.
[0007]
[Problem(s) to be Solved by the Invention] The conventional electronic formula frequency-selective

receiver constitutes the tuning circuit 2 from variable-capacitance-diode 2a as mentioned above. However, since said variable-capacitance-diode 2a is semi-conductor capacity, Q at the time of resonance becomes low, and the effectiveness of an antenna 1 has the problem of falling. Moreover, since, as for said variable-capacitance-diode 2a, the variable-capacity range was also decided the top where capacity value is small, the decision of the inductance of said antenna 1 has the problem that it is restricted greatly, by the received frequency range. .

[0008] For example, in the electronic formula frequency-selective receiver which can receive the standard wave of a long wave in Japan and Britain, JG2AS of Japan is [transmit frequencies] 40kHz, and MSF of Britain is [transmit frequencies] 60kHz. Therefore, as an electric wave, a frequency is low and the inductance value of said antenna 1 and the capacity value of a tuning circuit 2 become large. Since the transmit-frequencies ratio of Japan and Britain is 1.5 times at this time, if the large variable-capacity range of said variable-capacitance-diode 2a cannot be taken, the value of the inductance of said antenna 1 will become large. For this reason, naturally, said antenna 1 becomes large and a big limit will be given to the miniaturization of a receiver.

[0009] This invention aims at solving the technical problem that the miniaturization of an antenna 1 is difficult and the high tuning circuit 2 of Q is not obtained in the conventional electronic formula frequency-selective receiver.

[0010]

[Means for Solving the Problem] This invention for solving the above-mentioned problem An antenna and the alignment means of this antenna, A local oscillation circuit, a frequency changing circuit, and the superheterodyne method receiving circuit that has a demodulator circuit, In the electronic formula frequency complement receiver equipped with the electronic formula frequency complement means and frequency complement switch of a local oscillation circuit of this superheterodyne method receiving circuit By connecting said frequency complement switch between a reference potential and tuning capacitance By constituting so that selection connection of said tuning capacitance may be made at said alignment means, and connecting the node of said frequency complement switch and tuning capacitance to the control terminal of said electronic formula frequency complement means With a frequency complement switch, it is characterized by controlling an electronic formula frequency complement means.

[0011]

[Example] A drawing explains the example of this invention below. Drawing 1 gives the same number to the same element as the conventional example which is the block diagram of the electric-wave correction clock in which one example of the electronic formula frequency complement receiver of this invention is shown, and is shown in drawing 2 , and omits explanation. 12 consists of tuning capacitance 12a of immobilization, tuning capacitance 12b for selection connection, and frequency complement switch 12c in the tuning circuit. Parallel connection of said tuning capacitance 12a is carried out to an antenna 1, and where series connection is carried out, parallel connection of tuning capacitance 12b and the frequency complement switch 12c is carried out to said antenna 1. And the node of said tuning capacitance 12b and frequency complement switch 12c is connected to the reference potential VSS through pull down resistor 13a while connecting with the control terminal C of said electronic formula frequency complement means 6.

[0012] While connecting frequency complement switch 12c with VDD which is a reference potential among said tuning capacitance 12b like the above-mentioned configuration, frequency complement switch 12c and pull down resistor 13a constitute the frequency complement means 13 by connecting the node to the control terminal C of said electronic formula frequency complement means 6. That is, since the frequency complement signal S1 will be switched to VDD level through said frequency complement switch 12c if the frequency complement signal S1 serves as VSS level through pull down resistor 13a and frequency complement switch 12c will be in ON condition when frequency complement switch 12c is in the condition of OFF, corresponding to the level of these two reference potentials chosen, selection of the electronic formula frequency complement means 6 can be performed. That is, if MSF of Britain can receive and frequency selective ringing S1 switches to VDD when frequency selective ringing S1 is

VSS, it can choose so that JG2AS of Japan can be received. Moreover, when said pull down resistor 13a enlarges a value, it must be made for reduction of the input signal Ss which said frequency complement switch 12c leaks through said tuning capacitance 12b at the time of OFF to have to become the minimum.

[0013] 14 is the decoder circuit which inputs the detection signal DM of the output of said demodulator circuit 4, and decodes a time code, and outputs the time code signal TM. 15 is a time stamp means to display the time code signal TM of the output of said decoder circuit 14 as time-of-day data.

[0014] Next, actuation of the electric-wave correction clock of an example is explained. Reception actuation of JG2AS of Japan is explained first. If frequency complement switch 12c of the frequency complement means 13 is turned on, the frequency complement signal S1 will serve as VDD level. At this time, the electronic formula frequency complement means 6 chooses the Japanese frequency data D140 from the logical level of said frequency complement signal S1. And a control signal VC is generated according to said frequency data D140, said control signal VC is supplied to the anode of variable-capacitance-diode 5b of the local oscillation circuit 5, from the tank constant of capacitor 5c and coil 5a, the potential difference of the cathode which is VDD, and an anode determines capacity value, and said variable-capacitance-diode 5b is outputted [the oscillation frequency of the local oscillation circuit 5 is decided, and] as an office dispatch number LO which is the frequency of 140kHz. Said electronic formula frequency-selective means 6 inputs said station dispatch number LO here, and the frequency of said station dispatch number LO is compared with said frequency data D140. If the frequency from a station of the station dispatch number LO is lower than the frequency of the frequency data D140, the potential of said control signal VC will be lowered, and the cathode of said variable-capacitance-diode 5b and the potential difference of an anode become large, and they are controlled so that capacity value is made small and the oscillation frequency of the local oscillation circuit 5 becomes high. Moreover, if the frequency from a station of the station dispatch number LO is higher than the frequency of the frequency data D140, the potential of said control signal VC will be raised, and the cathode of said variable-capacitance-diode 5b and the potential difference of an anode become small, and they are controlled so that capacity value is enlarged and the oscillation frequency of the local oscillation circuit 5 becomes low. Thus, the frequency from a station of the station dispatch number LO of the local oscillation circuit 5 is controlled to be stabilized in accordance with the frequency data D140 of the electronic formula frequency complement means 6, and serves as a 140kHz signal with a very sufficient frequency precision. Since frequency complement switch 12c of said frequency complement means 13 is ON at this time, parallel connection of said tuning capacitance 12a and said tuning capacitance 12b is carried out, and the tuning frequency of 40kHz is decided by tuning capacitance 12a, the sum total capacity value of tuning capacitance 12b, and the inductance of said antenna 1.

[0015] An electric-wave signal with a tuning frequency of 40kHz efficiently received by said antenna 1 and alignment means 12 is inputted into said frequency changing circuit 3 as an input signal Ss. By the frequency changing circuit 3, on the frequency from a station of 140kHz of said station dispatch number LO, frequency conversion of said input signal Ss is carried out, and it is outputted as said intermediate frequency signal IF with an intermediate frequency of 100kHz, and it is detected in said demodulator circuit 4 designed only for detection with an intermediate frequency of 100kHz, and is outputted as a recovery signal DM. This recovery signal DM is decoded by the time code signal TM by said decoder circuit 14, and expresses this time code signal TM as the time stamp means 15 as time-of-day data.

[0016] Next, reception actuation of MSF of Britain is explained. If frequency complement switch 12c of said frequency complement means 13 is turned off, the frequency complement signal S1 will serve as VSS level through pull down resistor 13a. At this time, the electronic formula frequency complement means 6 chooses the British frequency data D160 from the logical level of said frequency complement signal S1. And a control signal VC is generated according to said frequency data D160, said control signal VC is supplied to the anode of variable-capacitance-diode 5b of the local oscillation circuit 5, from the tank constant of capacitor 5c and coil 5a, the potential difference of the cathode which is VDD, and an anode determines capacity value, and said variable-capacitance-diode 5b is outputted [the oscillation frequency of the local oscillation circuit 5 is decided, and] as an office dispatch number LO

which is the frequency of 160kHz. Said electronic formula frequency-selective means 6 inputs said station dispatch number LO here, and the frequency of said station dispatch number LO is compared with said frequency data D160. If the frequency from a station of the station dispatch number LO is lower than the frequency of the frequency data D160, the potential of said control signal VC will be lowered, and the cathode of said variable-capacitance-diode 5b and the potential difference of an anode become large, and they are controlled so that capacity value is made small and the oscillation frequency of the local oscillation circuit 5 becomes high. Moreover, if the frequency from a station of the station dispatch number LO is higher than the frequency of the frequency data D160, the potential of said control signal VC will be raised, and the cathode of said variable-capacitance-diode 5b and the potential difference of an anode become small, and they are controlled so that capacity value is enlarged and the oscillation frequency of the local oscillation circuit 5 becomes low. Thus, the frequency from a station of the station dispatch number LO of the local oscillation circuit 5 is controlled to be stabilized in accordance with the frequency data D160 of the electronic formula frequency complement means 6, and serves as a 160kHz signal with a very sufficient frequency precision. Since frequency complement switch 12c of said frequency complement means 13 is OFF at this time, the VDD side leaves said tuning capacitance 12b, and the tuning frequency of 60kHz is decided by the capacity value of tuning capacitance 12a, and the inductance of said antenna 1.

[0017] An electric-wave signal with a tuning frequency of 60kHz received efficiently is inputted into said frequency changing circuit 3 by the alignment means 12 as an input signal Ss with said antenna 1. By the frequency changing circuit 3, on the frequency from a station of 160kHz of said station dispatch number LO, frequency conversion of said input signal Ss is carried out, and it is outputted as said intermediate frequency signal IF with an intermediate frequency of 100kHz, and it is detected in said demodulator circuit 4 designed only for detection with an intermediate frequency of 100kHz, and is outputted as a recovery signal DM. This recovery signal DM is decoded by the time code signal TM by said decoder circuit 14, and expresses this time code signal TM as the time stamp means 15 as time-of-day data.

[0018] Therefore, by the electric-wave correction clock of said example, since the fixed capacity from which high resonance of Q is obtained can be used and a variable-capacity value is also determined by said tuning capacitance 12b, without catching said tuning capacitance 12a and said tuning capacitance 12b of said alignment means 12 by semi-conductor capacity, the degree of freedom of a design of the value of the inductance of said antenna 1 becomes [the degree of freedom of a design] large greatly.

[0019] Moreover, it is the tuning circuit 22, the antenna 1, and the block diagram of the frequency complement means 13 in which, as for drawing 3 , tuning capacitance and the location of a frequency complement switch show the example which put in and changed to drawing 1 , and said tuning circuit 22 consists of tuning capacitance 22a of immobilization, tuning capacitance 22b for selection connection, and frequency complement switch 22c. Parallel connection of said tuning capacitance 22a is carried out to an antenna 1, and where series connection is carried out, parallel connection of tuning capacitance 22b and the frequency complement switch 22c is carried out to said antenna 1. That is, in drawing 3 , it connects with a reference potential VDD and gets down from said tuning capacitance 22b, and the node of said tuning capacitance 22b and frequency complement switch 22c is connected to the reference potential VSS through pull down resistor 13a while connecting with the control terminal C of said electronic formula frequency complement means 6. While connecting said tuning capacitance 22b with VDD which is a reference potential among said frequency complement switch 22c, frequency complement switch 22c and pull down resistor 13a constitute the frequency complement means 13 by connecting the node to the control terminal C of said electronic formula frequency complement means 6. Namely, when frequency complement switch 22c is in the condition of OFF, the frequency complement signal S1 serves as VSS level through pull down resistor 13a. Moreover, since the frequency complement signal S1 will be switched to VDD level through said antenna 1 and frequency complement switch 22c if frequency complement switch 22c will be in ON condition Corresponding to the level of these two reference potentials chosen, selection of the electronic formula frequency-selective means 6 can be performed, and the tuning circuit 12 of above-mentioned drawing 1 and the function of

equivalence are achieved.

[0020]

[Effect of the Invention] As mentioned above, the frequency complement signal S1 is determined by the electronic formula frequency complement receiver of this invention turning on the frequency complement switch of said frequency complement means, and turning off, and said electronic formula frequency complement means can determine the existence of connection of tuning capacitance while choosing frequency data. At this time, since the tuning capacitance of the immobilization in said alignment means and the tuning capacitance for selection do not receive a limit of capacity value like [at the time of variable-capacitance-diode use], they can also design the value of the inductance of said antenna freely, and since they do not cause degradation of Q at the time of resonance, they can attain an efficient alignment means. Moreover, since the value of the inductance of an antenna can also be designed freely, the miniaturization of an antenna is also expectable. Moreover, since a switch of frequency selective ringing and a switch of said alignment means can be performed with one frequency complement frequency complement switch, there is also little number of a switch.

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12)**公開特許公報（Ａ）**　(11)特許出願公開番号

特開平6－125280

(43)公開日　平成６年(1994)５月６日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０４Ｂ　1/18		Ｊ　9298－5Ｋ		

審査請求　未請求　請求項の数１(全　６　頁)

(21)出願番号　特願平4－299369

(22)出願日　平成４年(1992)10月12日

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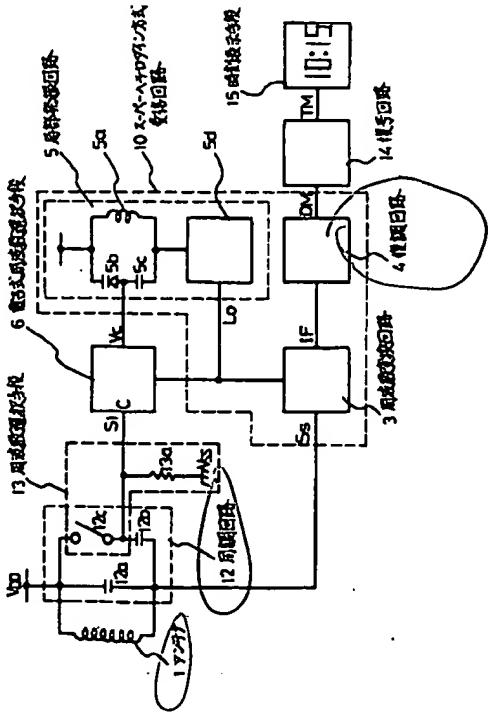
(54)【発明の名称】　電子式周波数選択受信機

(57)【要約】

【目的】　本発明は、電子式周波数選択受信機において１つの周波数選択スイッチの切り換えで、アンテナの同調容量の切り換えに周波数選択手段の切り換えとを同時に行なうことを目的としている。

【構成】　前記周波数選択スイッチのＯＮ／ＯＦＦにより前記同調容量の並列接続数を切替えて容量値を変化させることにより同調周波数を調整するとともに、アンテナの一端の電位を前記周波数選択スイッチのＯＮ時の電位と同電位として電子式周波数選択手段の制御端子を前記周波数選択スイッチのＯＮ時の電位として局発回路の周波数を選択する。

【効果】　同調容量を可変容量ダイオードでなく自由に選べるので、アンテナを含めて最適な設計が可能となる。



06/28/2004, EAST Version: 1.4.1

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【特許請求の範囲】

【請求項1】　アンテナと、該アンテナの同調手段と、局部発振回路と周波数変換回路と復調回路を有するスーパヘテロダイン方式受信回路と、該スーパヘテロダイン方式受信回路の局部発振回路の電子式周波数選択手段と、周波数選択スイッチとを備えた電子式周波数選択受信機において、前記周波数選択スイッチは、基準電位と同調容量間に接続されることにより、前記同調容量を前記同調手段に選択接続するよう構成され、かつ前記周波数選択スイッチと同調容量の接続点を前記電子式周波数選択手段の制御端子に接続したことを特徴とする電子式周波数選択受信機。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、電子式周波数選択受信機に関する。

【０００２】

【従来の技術】近年半導体技術やマイコン回路技術の目覚しい発展と、使用周波数帯の上昇にともない、受信回路のスーパヘテロダイン化が進んでいる。自動車電話に代表される移動体通信機はもちろん、ＴＶ、カーラジオ、ポータブルラジオ等、廉価版のものを除いてほとんどの受信機がデジィタルチューニングのスーパヘテロダイン方式の電子式周波数選択受信機となっている。前記電子式周波数選択受信機の一例としてＳＯＮＹ製のＰＬＬ　ＳＹＮＴＨＥＳＩＺＥＤ　ＲＥＣＥＩＶＥＲＩＣＦ－ＳＷ１があげられ、該ＩＣＦ－ＳＷ１は選局スイッチで周波数データを数値入力でき、大変便利に使用できる。

【０００３】ここで図２を用いて従来の電子式周波数選択受信機を説明する。図２は従来の電子式周波数選択受信機のブロック図で、１はアンテナで一端を電源プラス電位であるＶＤＤに接続し、電波信号をとらえ受信信号Ｓｓを発生する。２は同調回路であり容量値をアノード・カソード間の電圧レベルで制御可能な可変容量ダイオード２ａと、同調容量２ｂで構成され、前記可変容量ダイオード２ａと同調容量２ｂとは直列接続された状態で前記アンテナ１と並列接続されている。そして前記アンテナ１のインダクタンス値と同調回路２の容量値で、受信周波数である同調周波数ｆ１に同調している。３は前記受信信号Ｓｓを入力とし、もう一つの入力である局発信号ＬＯと混合して周波数変換し、中間周波数ｆ３の信号である中間周波数信号ＩＦを出力する周波数変換回路で、４は前記周波数変換回路３からの中間周波数信号ＩＦを入力して検波し、復調信号ＤＭを出力する復調回路である。５は局部発振回路であり、コイル５ａと、容量値をアノード・カソード間の電圧レベルで制御可能な可変容量ダイオード５ｂと、コンデンサ５ｃと、前記コイル５ａと可変容量ダイオード５ｂとコンデンサ５ｃとで構成されるタンク回路のタンク定数に従って発振する発振部５ｄとで構成されている。前記コイル５ａは一端をＶＤＤに接続するとともに一端を発振部５ｄに接続し、前記可変容量ダイオード５ｂと前記コンデンサ５ｃは直列接続された状態で前記コイル５ａと並列接続されている。発振部５ｄは前記タンク回路のタンク定数に従って発振した局発信号ＬＯを出力する。前記周波数変換回路３と、前記復調回路４と、前記局部発振回路５でスーパヘテロダイン方式受信回路１０を構成している。６は電子式周波数選択手段であり、基準電圧ＶＤＤはＶＳＳを周波数選択信号Ｓ１として入力し、その論理レベルにより周波数データを選択してその周波数データに対応する制御信号ＶＣを出力するとともに、前記局発信号ＬＯを入力することにより前記周波数データに従って前記制御信号ＶＣを安定させる。７は周波数選択手段で、一端をＶＤＤに接続し一端を前記電子式周波数選択手段６の制御端子Ｃに接続した周波数選択スイッチ７ａと、一端を電源マイナス電位であるＶＳＳに接続し一端を周波数選択スイッチ７ａに接続したプルダウン抵抗７ｂで構成されている。８はスピーカで復調信号ＤＭを可聴信号に変換する。

【０００４】次に図２を用いて従来の電子式周波数選択受信機の動作を説明する。例えば周波数選択手段７の周波数選択スイッチ７ａがＯＮしていると、周波数選択信号Ｓ１は周波数選択スイッチ７ａを介してＶＤＤレベルとなる。この時電子式周波数選択手段６は前記周波数選択信号Ｓ１の論理レベルから、周波数データＤ１を選択し、該周波数データＤ１に従って制御信号ＶＣを発生する。前記制御信号ＶＣは局部発振回路５の可変容量ダイオード５ｂのアノードに供給され、前記可変容量ダイオード５ｂはカソードに供給されるＶＤＤとアノードに供給される制御信号ＶＣとの電位差によって容量値を決定する。そして前記可変容量ダイオード５ｂとコンデンサ５ｃとコイル５ａとのタンク定数から、局部発振回路５の発振周波数が決まり局発信号ＬＯとして出力される。ここで前記電子式周波数選択手段６は前記局発信号ＬＯを入力することにより局発信号ＬＯの周波数と前記周波数データＤ１とを比較し、もし局発信号ＬＯの周波数ｆ２が周波数データＤ１の周波数よりも低ければ前記制御信号ＶＣの電位を下げることにより、前記可変容量ダイオード５ｂのカソードとアノードの電位差を大きくする方向に制御し、容量値を小さくして局部発振回路５の発振周波数が高くなるよう制御する。また局発信号ＬＯの周波数ｆ２が周波数データＤ１の周波数よりも高ければ前記制御信号ＶＣの電位を上げることにより、前記可変容量ダイオード５ｂのカソードとアノードの電位差を小さくする方向に制御し、容量値を大きくして局部発振回路５の発振周波数が低くなるよう制御する。このように局部発振回路５の局発信号ＬＯの局発周波数ｆ２は電子式周波数選択手段６の周波数データＤ１に一致し安定するよう制御されることにより、非常に精度の良い局部発

振回路５を供給できる．また前記制御信号ＶＣは前記同調回路２の前記可変容量ダイオード２ａのアノードにも供給されており、可変容量ダイオード２ａはＶＤＤの電位レベルにあるカソードと制御信号ＶＣの電位レベルにあるアノードとの電位差によって容量値を決定し、あらかじめ調整された前記同調容量２ｂの容量値と、前記アンテナ１のインダクタンスで同調周波数ｆ１が決まる．ここで前記局発信号ＬＯの局発周波数ｆ２と前記同調周波数ｆ１は常に中間周波数ｆ３と次式の関係にある．ｆ３＝ｆ２－ｆ１．よって同調周波数ｆ１は前記周波数データＤ１に依存する．

【０００５】前記アンテナ１と同調回路２によって効率良く受信された同調周波数ｆ１の電波信号は、受信信号Ｓｓとして前記周波数変換回路３へ入力される．周波数変換回路３で前記受信信号Ｓｓは前記局発信号ＬＯの周波数ｆ２で周波数変換され、中間周波数ｆ３の前記中間周波数信号ＩＦとして出力され、中間周波数ｆ３の検波専用に設計された前記復調回路４で検波されて復調信号ＤＭとして出力される．これが復調性能の優れたスーパヘテロダイン方式受信回路１０の特徴である．前記復調信号ＤＭは前記スピーカ８で可聴信号として発音される．

【０００６】以上のように従来の電子式周波数選択受信機では、操作の容易な周波数選択スイッチ７ａの切り換えによって、受信周波数同調が自動的に行え、非常に精度が良く安定した局部発振回路５を備えることにより、復調性能の優れたスーパヘテロダイン方式受信回路１０を実現している．

【０００７】

【発明が解決しようとする課題】以上のように従来の電子式周波数選択受信機は同調回路２を可変容量ダイオード２ａで構成している．しかし前記可変容量ダイオード２ａは半導体容量であるから共振時のＱは低くなりアンテナ１の効率は落ちるという問題がある．また前記可変容量ダイオード２ａは容量値が小さいうえ、その可変容量範囲も決まっているので受信周波数範囲によって前記アンテナ１のインダクタンスの決定は大きく制限されるという問題がある．．

【０００８】例えば長波の標準電波を日本とイギリスで受信できる電子式周波数選択受信機では、日本のＪＧ２ＡＳが送信周波数が４０ｋＨｚで、イギリスのＭＳＦが送信周波数が６０ｋＨｚである．よって電波としては周波数が低く、前記アンテナ１のインダクタンス値と同調回路２の容量値は大きくなる．このとき日本とイギリスの送信周波数比が１．５倍なので、前記可変容量ダイオード２ａの可変容量範囲を大きくとれないと前記アンテナ１のインダクタンスの値は大きくなる．このため当然前記アンテナ１は大きくなり、受信機の小型化に大きな制限を与えることになる．

【０００９】本発明は従来の電子式周波数選択受信機で

はアンテナ１の小型化が難しく、Ｑの高い同調回路２が得られないという課題を解決することを目的としている．

【００１０】

【課題を解決するための手段】上記問題を解決するための本発明は、アンテナと、該アンテナの同調手段と、局部発振回路と周波数変換回路と復調回路を有するスーパヘテロダイン方式受信回路と、該スーパヘテロダイン方式受信回路の局部発振回路の電子式周波数選択手段と、周波数選択スイッチとを備えた電子式周波数選択受信機において、前記周波数選択スイッチを基準電位と同調容量間に接続することにより、前記同調容量を前記同調手段に選択接続するよう構成し、かつ前記周波数選択スイッチと同調容量の接続点を前記電子式周波数選択手段の制御端子に接続することにより、周波数選択スイッチによって、電子式周波数選択手段を制御するようにしたことを特徴としている．

【００１１】

【実施例】以下図面により本発明の実施例を説明する．図１は本発明の電子式周波数選択受信機の一実施例を示す電波修正時計のブロック図であり図２に示す従来例と同一要素には同一番号を付し説明を省略する．１２は同調回路で固定の同調容量１２ａと、選択接続用の同調容量１２ｂと、周波数選択スイッチ１２ｃで構成されている．前記同調容量１２ａはアンテナ１に並列接続され、また同調容量１２ｂと周波数選択スイッチ１２ｃとは直列接続された状態にて前記アンテナ１に並列接続されている．そして前記同調容量１２ｂと周波数選択スイッチ１２ｃの接続点は前記電子式周波数選択手段６の制御端子Ｃに接続されるとともにプルダウン抵抗１３ａを介して基準電位ＶＳＳに接続されている．

【００１２】上記構成のごとく、周波数選択スイッチ１２ｃを基準電位であるＶＤＤと前記同調容量１２ｂ間に接続するとともに、その接続点を前記電子式周波数選択手段６の制御端子Ｃに接続することにより、周波数選択スイッチ１２ｃとプルダウン抵抗１３ａとが周波数選択手段１３を構成している．すなわち周波数選択スイッチ１２ｃがＯＦＦの状態にあるときはプルダウン抵抗１３ａを介して周波数選択信号Ｓ１はＶＳＳレベルとなっており、また周波数選択スイッチ１２ｃがＯＮ状態になると前記周波数選択スイッチ１２ｃを介して周波数選択信号Ｓ１がＶＤＤレベルに切り換えられるので、この選択される２つの基準電位のレベルに対応して電子式周波数選択手段６の選択がおこなわれるようにすることができる．すなわち周波数選択信号Ｓ１がＶＳＳのときはイギリスのＭＳＦが受信でき、また周波数選択信号Ｓ１がＶＤＤに切り換わると日本のＪＧ２ＡＳが受信できるように選択することができる．また前記プルダウン抵抗１３ａは値を大きくすることにより、前記周波数選択スイッチ１２ｃがＯＦＦ時に前記同調容量１２ｂを介してリー

クする受信信号Ｓｓの減少が最小限になるようにしなければならない。

【００１３】１４は前記復調回路４の出力の検波信号ＤＭを入力してタイムコードを復号する復号回路で、タイムコード信号ＴＭを出力する。１５は前記復号回路１４の出力のタイムコード信号ＴＭを時刻データとして表示する時刻表示手段である。

【００１４】次に実施例の電波修正時計の動作を説明する。まず日本のＪＧ２ＡＳの受信動作を説明する。周波数選択手段１３の周波数選択スイッチ１２ｃをＯＮすると、周波数選択信号Ｓ１はＶＤＤレベルとなる。この時電子式周波数選択手段６は前記周波数選択信号Ｓ１の論理レベルから、日本の周波数データＤ１４０を選択する。そして前記周波数データＤ１４０に従って制御信号ＶＣを発生し、前記制御信号ＶＣは局部発振回路５の可変容量ダイオード５ｂのアノードに供給され、前記可変容量ダイオード５ｂはＶＤＤであるカソードとアノードの電位差によって容量値を決定し、コンデンサ５ｃとコイル５ａとのタンク定数から、局部発振回路５の発振周波数が決まり周波数１４０ｋＨｚの局発信号ＬＯとして出力される。ここで前記電子式周波数選択手段６は前記局発信号ＬＯを入力し、前記局発信号ＬＯの周波数は前記周波数データＤ１４０と比較され、もし局発信号ＬＯの局発周波数が周波数データＤ１４０の周波数よりも低ければ前記制御信号ＶＣの電位を下げ、前記可変容量ダイオード５ｂのカソードとアノードの電位差は大きくなり、容量値を小さくして局部発振回路５の発振周波数が高くなるよう制御する。また局発信号ＬＯの局発周波数が周波数データＤ１４０の周波数よりも高ければ前記制御信号ＶＣの電位を上げ、前記可変容量ダイオード５ｂのカソードとアノードの電位差は小さくなり、容量値を大きくして局部発振回路５の発振周波数が低くなるよう制御する。このように局部発振回路５の局発信号ＬＯの局発周波数は電子式周波数選択手段６の周波数データＤ１４０に一致し安定するよう制御され、１４０ｋＨｚの非常に周波数精度の良い信号となる。この時、前記周波数選択手段１３の周波数選択スイッチ１２ｃはＯＮであるから、前記同調容量１２ａと前記同調容量１２ｂは並列接続され、同調容量１２ａと同調容量１２ｂの合計容量値と、前記アンテナ１のインダクタンスで同調周波数４０ｋＨｚが決まる。

【００１５】前記アンテナ１と同調手段１２によって効率良く受信された同調周波数４０ｋＨｚの電波信号は、受信信号Ｓｓとして前記周波数変換回路３へ入力される。周波数変換回路３で前記受信信号Ｓｓは前記局発信号ＬＯの局発周波数１４０ｋＨｚで周波数変換され、中間周波数１００ｋＨｚの前記中間周波数信号ＩＦとして出力され、中間周波数１００ｋＨｚの検波専用に設計された前記復調回路４で検波されて復調信号ＤＭとして出力される。該復調信号ＤＭは前記復号回路１４でタイムコード信号ＴＭに復号され、該タイムコード信号ＴＭは時刻表示手段１５で時刻データとして表示する。

【００１６】次にイギリスのＭＳＦの受信動作を説明する。前記周波数選択手段１３の周波数選択スイッチ１２ｃをＯＦＦすると、プルダウン抵抗１３ａを介して周波数選択信号Ｓ１はＶＳＳレベルとなる。この時電子式周波数選択手段６は前記周波数選択信号Ｓ１の論理レベルから、イギリスの周波数データＤ１６０を選択する。そして前記周波数データＤ１６０に従って制御信号ＶＣを発生し、前記制御信号ＶＣは局部発振回路５の可変容量ダイオード５ｂのアノードに供給され、前記可変容量ダイオード５ｂはＶＤＤであるカソードとアノードの電位差によって容量値を決定し、コンデンサ５ｃとコイル５ａとのタンク定数から、局部発振回路５の発振周波数が決まり周波数１６０ｋＨｚの局発信号ＬＯとして出力される。ここで前記電子式周波数選択手段６は前記局発信号ＬＯを入力し、前記局発信号ＬＯの周波数は前記周波数データＤ１６０と比較され、もし局発信号ＬＯの局発周波数が周波数データＤ１６０の周波数よりも低ければ前記制御信号ＶＣの電位を下げ、前記可変容量ダイオード５ｂのカソードとアノードの電位差は大きくなり、容量値を小さくして局部発振回路５の発振周波数が高くなるよう制御する。また局発信号ＬＯの局発周波数が周波数データＤ１６０の周波数よりも高ければ前記制御信号ＶＣの電位を上げ、前記可変容量ダイオード５ｂのカソードとアノードの電位差は小さくなり、容量値を大きくして局部発振回路５の発振周波数が低くなるよう制御する。このように局部発振回路５の局発信号ＬＯの局発周波数は電子式周波数選択手段６の周波数データＤ１６０に一致し安定するよう制御され、１６０ｋＨｚの非常に周波数精度の良い信号となる。この時、前記周波数選択手段１３の周波数選択スイッチ１２ｃはＯＦＦであるから、前記同調容量１２ｂはＶＤＤ側が離れ、同調容量１２ａの容量値と、前記アンテナ１のインダクタンスで同調周波数６０ｋＨｚが決まる。

【００１７】前記アンテナ１で同調手段１２によって効率良く受信された同調周波数６０ｋＨｚの電波信号は、受信信号Ｓｓとして前記周波数変換回路３へ入力される。周波数変換回路３で前記受信信号Ｓｓは前記局発信号ＬＯの局発周波数１６０ｋＨｚで周波数変換され、中間周波数１００ｋＨｚの前記中間周波数信号ＩＦとして出力され、中間周波数１００ｋＨｚの検波専用に設計された前記復調回路４で検波されて復調信号ＤＭとして出力される。該復調信号ＤＭは前記復号回路１４でタイムコード信号ＴＭに復号され、該タイムコード信号ＴＭは時刻表示手段１５で時刻データとして表示する。

【００１８】よって前記実施例の電波修正時計では前記同調手段１２の前記同調容量１２ａと前記同調容量１２ｂは、半導体容量にとらわれることなくＱの高い共振が得られる固定容量を使用することができ、また可変容量

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値も前記同調容量１２ｂによって決定されるので、設計の自由度が広く前記アンテナ１のインダクタンスの値も設計の自由度が大きくなる。

【００１９】また図3は図１に対して同調容量と周波数選択スイッチの位置がいれかわった実施例を示す同調回路２２とアンテナ１と周波数選択手段１３のブロック図で、前記同調回路２２は固定の同調容量２２ａと、選択接続用の同調容量２２ｂと、周波数選択スイッチ２２ｃで構成されている。前記同調容量２２ａはアンテナ１に並列接続され、また同調容量２２ｂと周波数選択スイッチ２２ｃとは直列接続された状態にて前記アンテナ１に並列接続されている。すなわち図３では前記同調容量２２ｂは基準電位ＶＤＤに接続されおり、また前記同調容量２２ｂと周波数選択スイッチ２２ｃの接続点は前記電子式周波数選択手段６の制御端子Ｃに接続されるとともにプルダウン抵抗１３ａを介して基準電位ＶＳＳに接続されている。前記同調容量２２ｂを基準電位であるＶＤＤと前記周波数選択スイッチ２２ｃ間に接続するとともに、その接続点を前記電子式周波数選択手段６の制御端子Ｃに接続することにより、周波数選択スイッチ２２ｃとプルダウン抵抗１３ａとが周波数選択手段１３を構成している。すなわち周波数選択スイッチ２２ｃがＯＦＦの状態にあるときはプルダウン抵抗１３ａを介して周波数選択信号Ｓ１はＶＳＳレベルとなっており、また周波数選択スイッチ２２ｃがＯＮ状態になると前記アンテナ１と周波数選択スイッチ２２ｃを介して周波数選択信号Ｓ１がＶＤＤレベルに切り換えられるので、この選択される２つの基準電位のレベルに対応して電子式周波数選択手段６の選択がおこなわれるようにすることができ、前述の図１の同調回路１２と等価の機能をはたす。

【００２０】

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【発明の効果】以上のように本発明の電子式周波数選択受信機は、前記周波数選択手段の周波数選択スイッチをＯＮ、ＯＦＦすることにより周波数選択信号Ｓ１が決定し、前記電子式周波数選択手段は周波数データを選択するとともに、同調容量の接続の有無を決定できる。この時前記同調手段における固定の同調容量と選択用の同調容量は、可変容量ダイオード使用時のような容量値の制限を受けないので前記アンテナのインダクタンスの値も自由に設計でき、共振時のQの劣化を招かないので効率の良い同調手段を達成することができる。またアンテナのインダクタンスの値も自由に設計できることからアンテナの小型化も期待できる。また周波数選択信号の切り換えと前記同調手段の切り換えを一つの周波数選択周波数選択スイッチでできるので、スイッチの個数も少ない。

【図面の簡単な説明】

【図１】本発明の電子式周波数選択受信機を示すブロック図である。

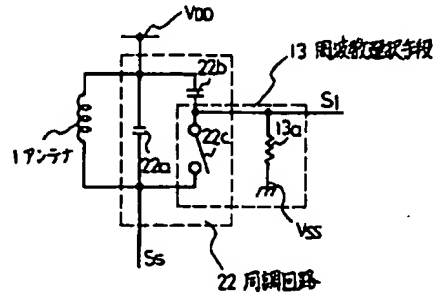
【図２】従来の電子式周波数選択受信機を示すブロック図である。

【図３】本発明の電子式周波数選択受信機の部品回路を示すブロック図である。

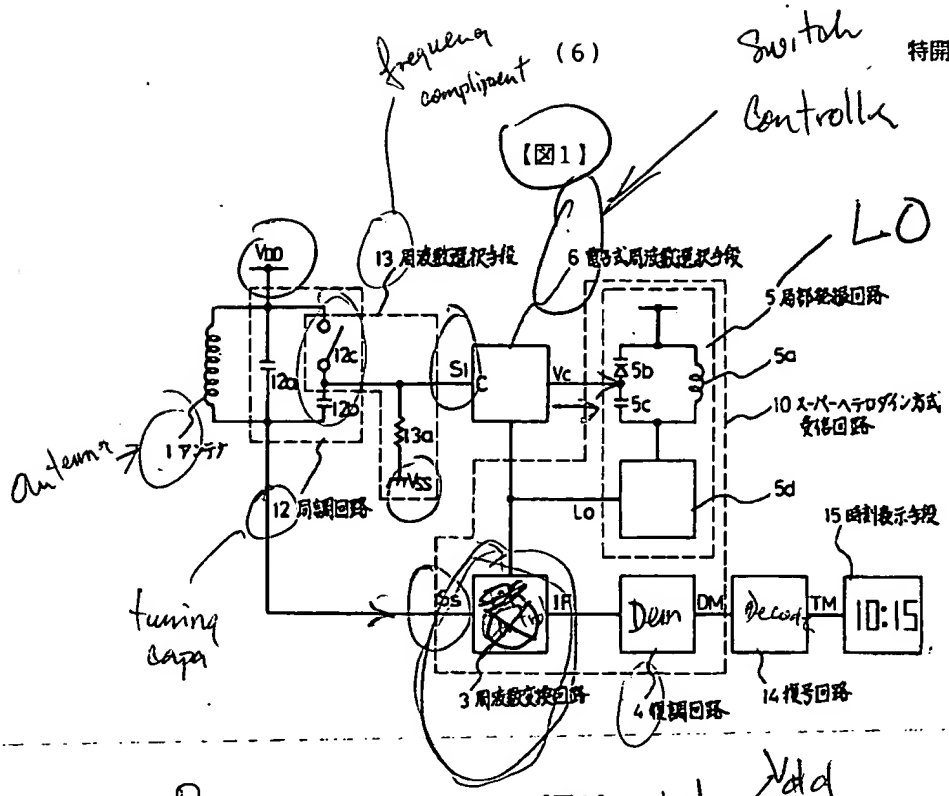
【符号の説明】

１　アンテナ
２、１２　同調回路
３　周波数変換回路
４　復調回路
５　局部発振回路
６　電子式周波数選択手段
７ａ、１２ｃ、２２ｃ　周波数選択スイッチ
１５　時刻表示手段

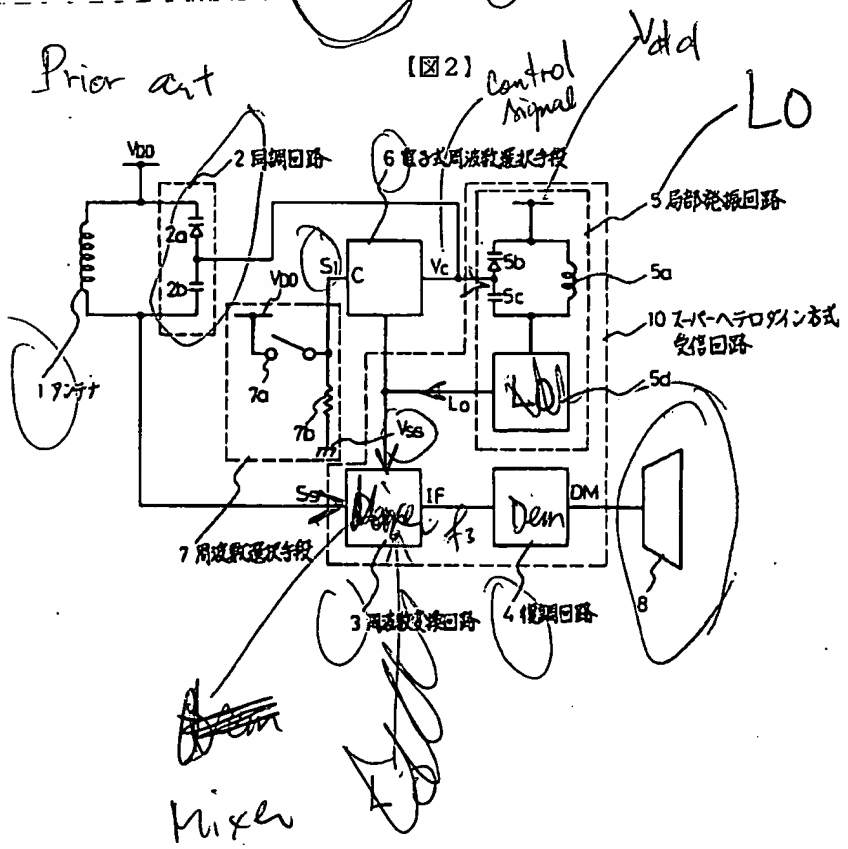
【図３】



【図1】


frequency complipent
Switch
Controlla
LO
VDD
13 周波数選択手段
6 直接式周波数選択手段
5 局部発振回路
12c
12a
12b
S1
C
Vc
5b
5c
5a
10 スーパーヘテロダイン方式受信回路
13a
Vss
Lo
5d
15 時計表示手段
antenna
1 アンテナ
12 同調回路
tuning capa
OSC
IF
Dem
DM
Decod
TM
10:15
3 周波数変換回路
4 復調回路
14 復号回路

【図2】


Prior art
Control signal
Vdd
LO
VDD
2 同調回路
6 直接式周波数選択手段
5 局部発振回路
2a
2b
S1
C
Vc
5b
5c
5a
10 スーパーヘテロダイン方式受信回路
1 アンテナ
7a
7b
Vss
Lo
5d
SSG
IF
Dem
DM
7 周波数選択手段
3 周波数変換回路
4 復調回路
8
Mixer